REMARKS

Election/Restrictions

The present application was subjected to a Restriction Requirement by the Examiner in the Restriction Requirement mailed on August 26, 2003. This Restriction Requirement restricted the present application to Group I, drawn to claims 1-2 and directed towards "a system with a non-volatile memory connected to a main memory bus, classified in class 711, subclass 103, and Group II, drawn to claims 3-26 and directed towards "a system utilizing flash memory, bi-directional connections and an SDRAM pin structure, among other features, classified in class 711, subclasses 101 and 103, and class 365." Applicant elected Group I, drawn to claims 1-2 in the Response filed on September 26, 2003. The Applicant added new claims 27-38 in the Response filed on March 3, 2004. Of the newly added claims 27-38, claims 27-33 depend from the original independent claim 1, and claims 35-38 depend from newly added independent claim 34. In the present Final Office Action of March 19, 2003, the Examiner maintained that newly submitted claims 27-33 and 35-38 are directed to the invention of non-elected claims of Group II and that therefore claims 27-33 and 35-38 were withdrawn from consideration.

As Applicant believes claims 1 or 34, as amended, to be generic to one or more of claims 2 and 27-38. Applicant notes that, should a generic claim be allowed, Applicant is entitled to consideration of claims to the other species of withdrawn claims 27-33 and 35-38, which are written in dependent form or otherwise include all the limitations of an allowed generic claim as provided by 37 CFR 1.141.

Duplicate Claims

In the present Final Office Action of March 19, 2003, the Examiner additionally maintained that newly submitted independent claim 34 is substantially duplicate of claim 2. The Examiner further maintained that if claim 2 was found allowable, claim 34 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof.

Applicant has amended claim 34 herein and respectfully submits that the scope of dependent claim 2 and independent claim 34 to be different. The Applicant therefore believes the prohibition of duplicate claims under 37 CFR 1.75 to be satisfied.

Drawing Rejection under U.S.C. § 1.83(a)

The drawings were objected to under 37 CFR 1.83(a), as informal and not proper margins. Substitute drawings are submitted herewith. The Applicant respectfully maintains that the substitute drawings conform to the requirements of 37 CFR 1.83(a) and introduce no new matter. The Applicant therefore requests Examiner approval of the substitute drawings and withdrawal of the objection under 37 CFR 1.83(a).

Rejections Under 35 U.S.C. § 102

Claims 1, 2 and 34 were rejected under 35 U.S.C. § 102(b) as being anticipated by Bacon et al. (U.S. Patent 5,440,632). Applicant respectfully traverses this rejection and feels that claims 1-2 and 34 are allowable for the following reasons.

Applicant disagrees with the Examiner and respectfully maintains that Bacon et al. teaches a Flash memory for a reprogrammable subscriber service having a control microprocessor 128, a memory bus 141, and an asynchronous Flash EPROM 134 coupled to the memory bus 141.

The Examiner stated in the Final Office Action mailed March 19, 2003, that, "the data transfers to the Flash EPROM in the Bacon et al. system are clearly shown to be synchronous."

The Applicant notes that nowhere does Bacon et al. specifically disclose that its Flash or EPROM is synchronous or has a synchronous interface. The Applicant disagrees with the assertion that a system containing a synchronous component or a system with a memory that accepts a clock signal means that the memory of the system is inherently a memory of a synchronous type and has a synchronous type of interface. Applicant respectfully submits that if the Examiner maintains that this an inherent feature, the Examiner has the burden of proving that the inherent element must of

necessity only work in the manner of the Applicant's disclosed invention. If any other interpretation is possible for the inherent element relied upon for the rejection, the rejection cannot be maintained. "To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.'" In re Robertson, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999) (citations omitted); (*See,* MPEP §2112 and §2163.07(a)). "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." *Ex parte Levy*, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original). (*See,* MPEP §2112).

Applicant respectfully submits that the allegedly inherent characteristic of a synchronous non-volatile memory system does not necessarily flow from the teachings of the applied prior art of Bacon et al. and would be so recognized by persons of ordinary skill. In other words, that a system containing a synchronous component or a system with a memory that accepts a clock signal necessarily implies that the memory of the system is inherently a memory of a synchronous type and has a synchronous type of interface. Applicant also submits that there are multiple possible interpretations for the fact that the memory system has a synchronous component or has a memory that accepts a clock signal, besides the conclusion that the memory of the system is inherently a memory of a synchronous type and/or has a synchronous type of interface.

A system is not synchronous because it is tied to a clocked processor. If so, all memory would be considered synchronous.

One possible alternative interpretation is that the memory of Bacon et al. interfaces to an external system that has a synchronous RF audio signal (a television signal that time-wise multiplexes video and audio) and therefore must have a synchronous detector as a component to detect and isolate the audio component of the signal. As such, because of the fact that a person of ordinary skill in the art would not

recognize that the system of Bacon et al. would necessarily be a synchronous memory system or contain a synchronous memory device, and that there are multiple possible interpretations to the system of Bacon et al. having a synchronous non-memory component or a memory that accepts a clock, the Examiner has not shown the necessity required for inherency in claiming Bacon et al. describes a synchronous non-volatile memory system or having a synchronous non-volatile memory. Therefore as Bacon et al. does not inherently describe a synchronous non-volatile memory system or having a synchronous non-volatile memory, the Applicant submits that Bacon et al. fails the all element rule for Applicant's independent claims 1 and 34, as amended.

Applicant also submits that if the Examiner maintains that Bacon et al. inherently describes a synchronous non-volatile memory system or as inherently having a synchronous non-volatile memory, that such inherency may be rebutted by the Applicant by the submission of extrinsic evidence to the contrary. A *prima facie* case of inherency by the Patent Office may be rebutted by the Applicant by an appropriate showing. "When the PTO shows a sound basis for believing that the products of the applicant and the prior art are the same, the applicant has the burden of showing that they are not." *In re Spada*, 911 F.2d 705, 709, 15 USPQ2d 1655, 1658 (Fed. Cir. 1990). (*See,* MPEP §2112.01). In supporting or rebutting an inherent element, extrinsic evidence may be relied upon for inherent elements are considered as such in light of the ordinary person skilled in the art would know or assume. Extrinsic evidence may be used to explain but not expand the meaning of terms and phrases used in the reference relied upon as anticipatory of the claimed subject matter. *In re Baxter Travenol Labs*, 952 F.2d 388, 21 USPQ2d 1281 (Fed. Cir. 1991); (*See*, MPEP §2131.01, II).

Applicant respectfully submits that the Application utilizes the term "synchronous" in claims 1-2 and 27-38 of the present application to refer to a memory type that incorporates a synchronous interface. In other words, a memory of a type where the interface has a defined timing and the data is placed on or read from the memory interface at a specified time during a data access interaction with the memory. Applicant submits that such is explained in the Application as originally filed. *See*, Application, Page 2, Lines 11-17. Applicant respectfully submits that a person of ordinary skill in the

art would interpret a synchronous memory device as meaning a memory device with a synchronous interface as described by Applicant above.

In support of this, Applicant recites the extrinsic evidence of Barth et al. (U.S. Patent 6,532,522, Titled: "Asynchronous request/synchronous data dynamic random access memory", Issued: March 11, 2003) to rebut the Examiner's argument of inherency and support the Applicant's claim that a person of ordinary skill in the art would interpret a synchronous memory device as meaning a memory device with a synchronous type interface. *See, e.g.,* Barth et al., column 1, lines 21-46, column 2, line 48 to column 3, line 3, and Figures 1, 2, 3 and 4. As such, Applicant submits that Barth et al. rebuts the Patent Office's assertion that Bacon et al. is inherently a system with a synchronous non-volatile (EPROM/Flash) memory and submits that one of ordinary skill in the art would recognize Bacon et al. as describing a non-synchronous memory.

In addition, the Applicant specifically responds to the portions of Bacon et al. raised by the Examiner as supportive of Bacon et al. disclosing a synchronous system. Regarding (a), the use of a synchronous detector 105 in column 7, line 7 of Bacon et al., the Applicant notes that the synchronous detector 105 is coupled to the RF detection path and input of the subscriber terminal of a subscription television system in FIG. 2 and is not directly coupled to the EROM/Flash 134 or microprocessor 128. The "audio signal is converted from the 41.25 Mhz IF carrier to the intermodulation frequency of 4.5 Hz by synchronous detector 105." *See, e.g.,* Bacon et al. Figures 2A and 2B, column 6, line 15 to column 7, line 28, and column 7, lines 5-7.

Regarding (b), the Examiner noted, "column 11, lines 45 et seq., which state 'The microprocessor 128 time multiplexes the port C lines to be both address and data lines AD0-A7 and applies the to a data latch 202 which maintains the address word while to reads data from the same lines. The address lines are applied to the address inputs A0-A15 of the internal memory 134, in FIG. 5 a 256k Flash EPROM (pages 0-3).' Time multiplexing is a synchronous activity." The Applicant maintains that, Bacon et al. column 11, lines 45 et seq. discloses a microprocessor coupled to an external latch 202, as shown in FIG. 5, that holds the lower portion of the address (A0-A7) to be accessed in the memory 134 so that the port C of the microprocessor 128 can be reused to transmit or

receive data to/from the memory 134. While this activity may be constrained to occur in a sequential fashion (load address in latch 202 to access a location in memory 134, read/write memory 134), the Applicant maintains that this does not state that the memory is synchronous or even that the interaction with the data latch and following access to the memory 134 occur in a synchronous manner; all that is required is that the data latch 202 be loaded with the lower portion of an address (A0-A7) before the memory 134 is accessed. In addition, the Applicant maintains that the statement "[t]he microprocessor 128 timewise multiplexes port C lines to be both address and data lines AD0-AD7 and applies them to data latch 202 which maintains the address word while it reads data from the same lines," only refers to the timewise dual use of the lines of microprocessor port C, and not that the interaction of the microprocessor 128 and memory 134 being synchronous. *See, e.g.*, Figure 5 and column 11, lines 45-59.

Regarding (c), the Examiner noted, "column 11, lines 63 et seq., which state 'An address clock on line ACLK provides a clock signal to synchronize the transfer of data between the microprocessor 128 and MCC 104." The Applicant maintains that, while this may indicate that data transfer between the microprocessor 128 and the multifunction control circuit (MCC) 104 of the subscriber system, this does not state or suggest that the memory 134 is a synchronous non-volatile memory or has a synchronous memory interface.

Regarding (d), the Examiner noted, "column 12, lines 18 et seq., which state 'The SMB comprises 4 input/output data lines SD0-SD3 and a serial clock line SCLK to time the communications. The memory controller 112 additionally provides a master clock.'" The Applicant notes that the secure microprocessor bus (SMB) 143 is not coupled to Flash EPROM 134 in FIG. 5 of Bacon et al., and is only shown coupled to the MCC 104, the secure microprocessor 136, and the memory extension connector 200. The Applicant maintains that this does not disclose that the memory 134 is a synchronous non-volatile memory or has a synchronous memory interface. Furthermore, the Applicant notes that Bacon et al. discloses SCLK is for serial clocking and that the expansion connector 200 allows another secure microprocessor 201 to be coupled to the SMB bus 143 to

supplement or override the secure microprocessor 136. *See, e.g.*, Figures 5 and 7, column 12, lines 16-22, lines 34-37, and column 12, line 62 to column 13, line 4.

Applicant therefore maintains that Bacon et al. teaches an asynchronous Flash EEPROM, and that therefore it does not teach or suggest a computer system comprising a memory controller, a main memory bus coupled to the memory controller, and a synchronous non-volatile memory device coupled to the main memory bus. *See, e.g.*, Bacon et al., Figures 2 and 5, and column 8, line 30-39, and column 12, lines 9-34.

Applicant's claim 1 is directed to a computer system comprising a memory controller, a main memory bus coupled to the memory controller, and a synchronous non-volatile memory device coupled to the main memory bus. As detailed above, Applicant submits that Bacon et al. fails to disclose such a system or a memory device. As such, Bacon et al. fails to teach all elements of independent claim 34.

Applicant's claim 34, as amended, is directed to a computer system comprising a memory controller, a main memory bus coupled to the memory controller, and a synchronous non-volatile memory device coupled to the main memory bus. The synchronous non-volatile memory having a command interface, where the command interface comprises a write enable connection (WE#) to receive a write enable signal, a column address strobe connection (CAS#) to receive a column address strobe signal, and a row address strobe connection (RAS#) to receive a row address strobe signal. As detailed above, Applicant submits that Bacon et al. fails to disclose such a system or a memory device. As such, Bacon et al. fails to teach all elements of independent claim 34.

Applicant respectfully contends that claims 1 and 34 have been shown to be patentably distinct from the cited reference. As claim 2 depends from and further defines claim 1, it is also considered to be in condition for allowance. Accordingly, Applicant respectfully requests allowance of claims 1-2 and 34.

Entry of Withdrawn Claims upon Allowance of a Generic Claim

The Applicant respectfully requests entry of withdrawn claims 27-33 and 35-38 upon allowance of generic claims 1 and 34.

CONCLUSION

In view of the above remarks, Applicant respectfully submits that the claims are in condition for allowance and requests reconsideration of the application and allowance of the claims. No new matter has been added and no additional fee is required by this amendment and response.

The Examiner is invited to contact Applicant's representative at the number below if there are any questions regarding this response or if prosecution of this application may be assisted thereby.

Respectfully submitted,

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